Extrapolated $f_{\max}$ for Carbon Nanotube FETs

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Abstract. Compact expressions are derived for the maximum operating frequency of carbon nanotube field-effect transistors. The expressions are shown to be applicable over wide ranges of physical properties, parasitic resistances, and gate biases. The utility of the expressions is demonstrated by their prompting of a conservative device design that should lead to $f_{\max} > 0.5\,\mathrm{THz}$.

1. INTRODUCTION

The frequency $f_{\max}$, at which the extrapolated power gain becomes unity, is a well-established figure-of-merit for characterizing the high-frequency performance of transistors. A useful, compact expression for $f_{\max}$ is available for heterojunction bipolar transistors [1], but, in Si metal-oxide-semiconductor field-effect transistors, the need to consider the electrical properties of the substrate makes for a more complicated situation. However, in carbon nanotube field-effect transistors (CNFETs), the substrate is not an active part of the device, so the traditional, small-signal equivalent circuit, in which there are no elements representing the substrate [2, p.441], can be used as a basis for deriving a useful expression for $f_{\max}$. Moreover, because of the small size of CNFETs, the quasi-static approximation should be valid up to very high frequencies. Here, starting from the small-signal parameters of the equivalent circuit, we systematically make a series of approximations that lead to compact expressions for the extrapolated $f_{\max}$. These expressions are shown to be applicable over a wide range of conditions, and to be useful in guiding the design of high-frequency devices.

2. MODELING PROCEDURES

The small-signal, extrinsic z-parameters for the equivalent circuit shown in Fig. 1 are given by the standard expressions [2, p.440]:

$$\begin{aligned} z_{11e} &= y_{22}/Y + R_{sg} \\ z_{12e} &= -y_{12}/Y + R_s \\ z_{21e} &= -y_{21}/Y + R_s \\ z_{22e} &= y_{11}/Y + R_{sd} \\ Y &= y_{11}y_{22} - y_{12}y_{21}\ , \end{aligned} \tag{1}$$

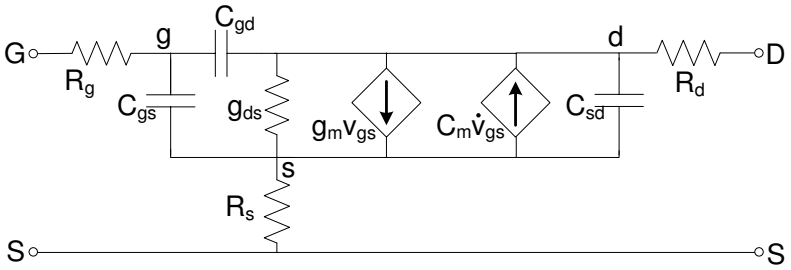

Figure 1. Small-signal equivalent circuit for the CNFET.

where $R_{sg} = R_s + R_g$, $R_{sd} = R_s + R_d$, and the intrinsic y-parameters are [3, p.378]:

$$\begin{aligned} y_{11} &= j\omega(C_{gs} + C_{gd}) \\ y_{12} &= -j\omega C_{gd} \\ y_{21} &= g_m - j\omega(C_m + C_{gd}) \\ y_{22} &= g_{ds} + j\omega(C_{sd} + C_{gd}) \ . \end{aligned} \tag{2}$$

The transcapacitance C_m relates non-reciprocal capacitance pairs, and is given by, for example, $C_{dg} - C_{gd}$. From the components in Eq. (1), an expression for the radian frequency ω_T at which the short-circuit, common-source, current gain reaches unity, when extrapolated from some lower frequency at which the gain rolls-off at -10 dB/decade, follows, namely [2, p.441]:

$$\frac{1}{\omega_T} = \frac{1}{\omega_t}[1 + g_{ds}R_{sd}] + R_{sd}C_{gd} \ , \tag{3}$$

where the intrinsic "cut-off" frequency is given by

$$\omega_t = \frac{g_m}{(C_{gs} + C_{gd})} \ . \tag{4}$$

The assumptions made in arriving at the expressions for the extrapolated unity-current-gain frequencies are that the frequency at which the extrapolation can properly begin is subject to the following restrictions:

$$\omega^2 \ll g_m^2/(C_m + C_{gd})^2 \tag{5}$$

$$\omega^2 \ll g_m/(AR_s) \tag{6}$$

$$\omega^2 \ll g_m^2/(C_{dg} + BR_s)^2 \tag{7}$$

$$\omega^2 \ll (C_{gg} + BR_{sd})^2/(AR_{sd})^2 \ , \tag{8}$$

where

$$\begin{aligned} A &= C_{dg}C_{gd} - C_{gg}C_{dd} \\ B &= C_{gg}g_{ds} + C_{gd}g_m \\ C_{gg} &= C_{gs} + C_{gd} \\ C_{dd} &= C_{sd} + C_{gd} \ . \end{aligned}$$

The above limitations should easily be satisfied by CNFETs intended for operation at frequencies of several hundreds of GHz . For the power gain, we use Mason's unilateral gain [4]:

$$U = \frac{|z_{21e} - z_{12e}|^2}{4\left[\Re(z_{11e})\Re(z_{22e}) - \Re(z_{12e})\Re(z_{21e})\right]} \ . \tag{9}$$

One further restriction on the extrapolation frequency is required to obtain an expression for U with the desired dependence on ω^{-2}:

$$\omega^2 \ll B^2/A^2 \ . \tag{10}$$

In fact, Eq. (10) is a more stringent restriction than the fourth assumption of Eq. (8), which is, therefore, rendered redundant.

It follows, after lengthy algebraic manipulation, that U can be written in the form that is familiar for bipolar transistors [1]:

$$U = \frac{\omega_T}{4\omega^2 (RC)_{\text{eff}}} \ , \tag{11}$$

where $(RC)_{\text{eff}}$ is an effective time constant. Because the assumptions we wish to make in order to simplify the expression for $f_{\max}$ affect both ω_T and $(RC)_{\text{eff}}$ we elect not to isolate the expression for the latter [1], but, instead, to work on the expression for the reciprocal cyclic frequency τ_{eff}, where

$$\tau_{\text{eff}}^2 = \frac{(RC)_{\text{eff}}}{\omega_T} \ , \tag{12}$$

and

$$f_{\max} = \frac{1}{4\pi\tau_{\text{eff}}} \ . \tag{13}$$

With the assumptions made so far, τ_{eff} is given by

$$\begin{aligned} \tau_{\text{eff},1}^2 \quad = \quad & \tfrac{B}{g_m^2} \left\{ R_g (C_{gg} + 2R_c B) + R_c \left[C_{gg} - C_m \right.\right. \\ & \left.\left. + 2C_{sd} + R_c B + \tfrac{A}{B}(g_m + 2g_{ds}) \right] \right\} \ , \end{aligned} \tag{14}$$

where, for convenience, we have assumed similar source and drain contacts, and set $R_s = R_d = R_c$.

To make progress in simplifying Eq. (14), one has to compare component values, which, because of their bias- and device-dependence, cannot be expected to result in relations that are as generally applicable as the frequency limitations stated earlier in Eqs. (5)-(8) and (10). We start by asserting

$$C_{gs} = C_{gd} \ . \tag{15}$$

The motivations for doing this are the small size and longitudinal symmetry of CNFETs: the electrodes are inevitably very close together, so the extrinsic contributions to C_{gs} and C_{gd} will be significant; and the symmetry would make them equal. We can anticipate this equality breaking down at low- and high-gate bias, when the electrode-dependent quantum-capacitance contribution to C_{gs} and C_{gd}, respectively, is particularly significant [5]. Using Eq. (15) in Eq. (14) leads to a considerable simplification:

$$\tau_{\text{eff},2}^2 = \frac{C_{gd}^2}{g_m} \left(1 + \frac{2g_{ds}}{g_m} \right) (2R_g + R_c)[1 + R_c(g_m + 2g_{ds})] \ . \tag{16}$$

Finally, in the interests of further simplification, we suggest:

$$g_m \gg 2g_{ds} \ . \tag{17}$$

This inequality may break down in CNFETs with small-diameter (large-bandgap) nanotubes, for which the transconductance is generally less than in those with large-diameter tubes. The result of this additional assumption is a very compact expression:

$$\tau_{\text{eff},3}^2 = \frac{C_{gd}^2}{g_m} (2R_g + R_c)(1 + g_m R_c) \ . \tag{18}$$

In the next section we evaluate the validity of Eqs. (14), (16) and (18) for several Schottky-barrier CNFETs. The component values are evaluated as described previously [5], using a Schrödinger-Poisson solver [6], with the inclusion of the complex band structure of the nanotube [7]. We found that it was not necessary to consider more than the lowest, doubly-degenerate band for the tubes and bias ranges considered in this work.

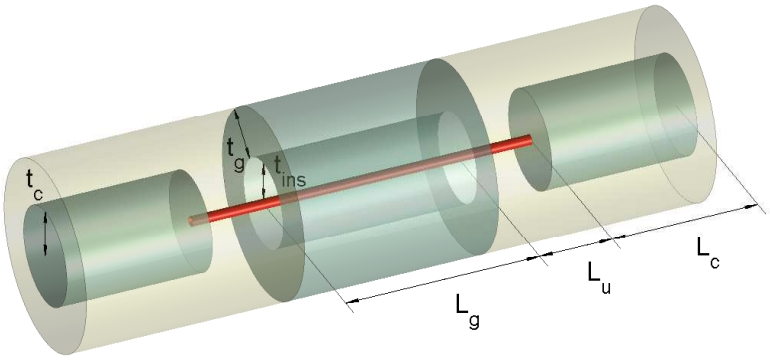

Figure 2. Coaxial CNFET structure. The insulator fills the entire simulation space not occupied by metal or the nanotube.

3. RESULTS AND DISCUSSION

In seeking ultimate performance limits we examine devices of the coaxial structure shown in Fig. 2, but we base values for the physical properties on those of presently realizable planar structures, such as a recent, high-DC-performance device [8]. All the devices considered here have a gate of length $L_g = 50\,\text{nm}$ and of thickness $t_g = 20\,\text{nm}$, an insulator relative permittivity of 16 (HfO_2), and Pd end-contacts of radius $t_c = 4\,\text{nm}$. Unless otherwise stated, the contact length is $L_c = 100\,\text{nm}$, the gate underlaps are $L_{us} = L_{ud} = 5\,\text{nm}$, and the contact resistances are computed from a Pd resistivity of $0.48\,\text{k}\Omega\cdot\text{nm}$, which can be inferred from Ref. [8]. The data of Ref. [9] was used for the tube-dependent, end-contact barrier heights, while the work function of the gate was set equal to that of the nanotube [10]. The latter assignment is arbitrary in view of the lack of information on other factors, such as oxide charge, that will affect the threshold voltage in practice, and serves only to change the effective gate potential. The gate resistance can be expected to have a large effect on $f_{\max}$ [11], but, in the present absence of knowledge about practical gate connection configurations, we take, unless otherwise stated, $R_g = 1\,\text{k}\Omega$. With the dimensions listed above, for example, $R_c \approx 0.9\,\text{k}\Omega$. The trends in the capacitances illustrated in Fig. 1 have been discussed previously [5, 12], and for the particular devices described here C_{gs} and C_{gd} are on the order of 10 aF.

Firstly, we consider Device 1, which has a nanotube diameter $d_t = 1.7\,\text{nm}$ (taken to correspond to a tube of chirality (22,0)), for which the Pd contacts produce a negative barrier for holes of $-0.04\,\text{eV}$ [9]. The combination of low barrier height and an insulator thickness of $t_{\text{ins}} = 2.5\,\text{nm}$ should produce a device of high transconductance. Mason's power gain U is shown in Fig. 3, from which it is clear that, for this particular

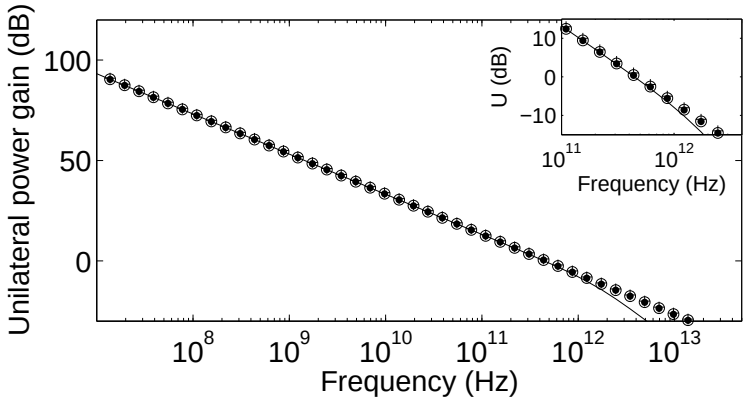

Figure 3. Unilateral power-gain for Device 1 using Eq. (9) (solid), and Eq. (11) with Eq. (14) (dots), Eq. (16) (circles), and Eq. (18) (crosses). The inset magnifies the curves near 0 dB. $V_{GS} = V_{DS} = -0.5\,\mathrm{V}$.

device at the given biases of $V_{GS} = V_{DS} = -0.5\,V$, all the assumptions leading to Eqs. (14), (16) and (18) are reasonable. The effects of the assumptions do appear, however, at different V_{GS}, as illustrated in Fig. 4. It can be seen that the lowest τ_{eff} is $\approx 0.16\,\mathrm{ps}$, which corresponds to $f_{\max} \approx 500\,\mathrm{GHz}$. At high, negative, gate bias, injection of holes from the drain is facilitated [11], leading to an increase in the quantum-capacitance contribution to C_{gd}. Thus, assumption Eq. (15) overestimates C_{gs}, leading to Eq. (16) overestimating the true τ_{eff} at the most negative bias considered. The effect of assumption Eq. (17) is more severe at high bias because g_m falls off considerably. Again, this is due to holes being injected into the nanotube from the drain: the resulting hole flow bucks that issuing from the source, reducing g_m. Moreover, g_{ds} rises in that bias range, ultimately yielding a ratio $2g_{ds}/g_m \approx 1$ near $V_{GS} = -0.8\,\mathrm{V}$ and invalidating assumption Eq. (17).

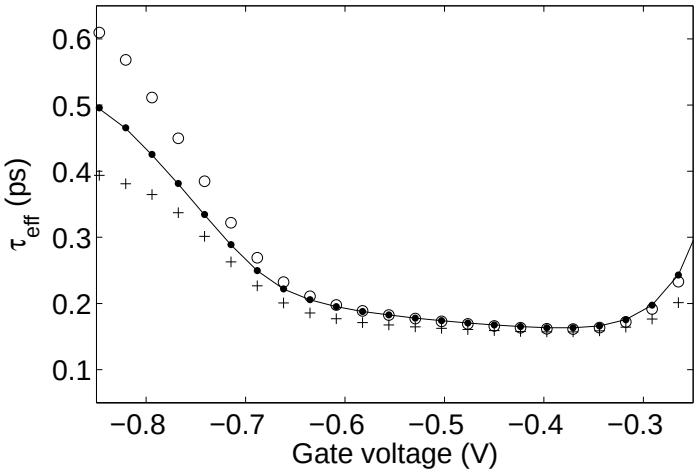

Figure 4. τ_{eff} estimates for Device 1 using Eq. (9) (solid), and Eq. (13) with Eq. (14) (dots), Eq. (16) (circles), and Eq. (18) (crosses). $V_{DS} = -0.5\,V$.

We turn now to Device 2, which has a nanotube diameter $d_t = 0.8\,\text{nm}$ (taken to correspond to a tube of chirality (10,0)), a positive hole-barrier of 0.3 eV at the Pd end-contacts [9], an increased insulator thickness t_{ins} of 8 nm and shorter contacts L_c of 30 nm. The higher barriers and thicker insulator will reduce g_m below that of Device 1. These features should lead to a lower $f_{\max}$ than predicted for Device 1. However, this should be mitigated somewhat by lower capacitances C_{gs} and C_{gd}, due to the larger t_{ins} and smaller L_c. The results shown in Fig. 5 show that $f_{\max}$ is, indeed, significantly lower than for Device 1. Interestingly, $\tau_{\text{eff},2}$ is a better approximation to the true τ_{eff} in this case, which is perhaps unexpected, given that the shorter L_c and thicker t_{ins} should reduce the inter-electrode capacitances that would otherwise help to equalize C_{gs} and C_{gd}. The reason lies in the positive barrier heights and larger bandgap, which restrain charge injection into the nanotube (see inset to Fig. 5), thereby reducing the quantum capacitance contributions to C_{gs} and C_{gd} even more than the above physical changes reduce the inter-electrode contributions. The higher barrier at the source generally reduces the drain current, so both g_m and g_{ds} are affected, and $\tau_{\text{eff},3}$ is no worse an approximation, relatively speaking, than it was for Device 1.

One of the reasons for the low $f_{\max}$ shown for Device 2 in Fig. 5 is that the effective gate bias is lower than for Device 1 because of the higher threshold voltage due to the thicker gate insulator. While this could be ameliorated by application of a higher negative bias to the gate, or by using a higher work function for the gate metal, Fig. 5 is useful because it illustrates that our equations are reasonable over an effectively different bias range than applies to Device 1.

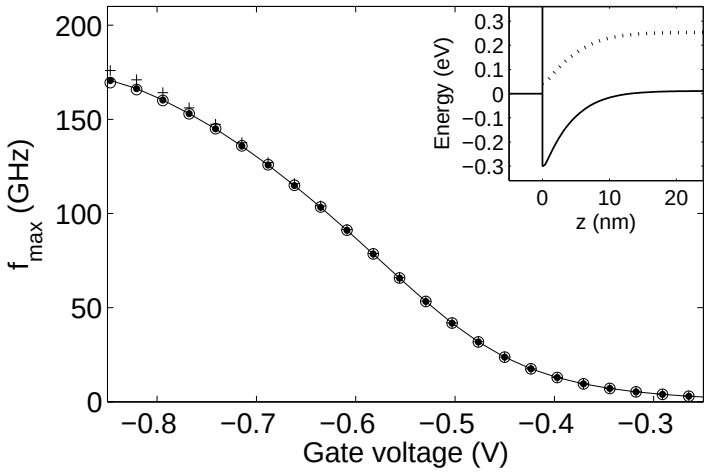

Figure 5. $f_{\max}$ estimates for Device 2, at $V_{DS} = -0.5\,\text{V}$, using Eq. (9) (solid) and Eq. (13) with Eq. (14) (dots), Eq. (16) (circles), and Eq. (18) (crosses). The inset illustrates the valence band edge profiles near the source contact for Devices 1 (dotted) and 2 (solid) at $V_{GS} = V_{DS} = -0.5\,\text{V}$. Energies are referenced to the source Fermi level.

So far, we have used resistances of $R_c \approx 0.9\,\text{k}\Omega$ and $\approx 0.3\,\text{k}\Omega$ for Devices 1 and 2, respectively, and $R_g = 1\,\text{k}\Omega$. To examine the effect of parametrically changing these values, results are presented in Fig. 6 for Device 1. The error in the estimation of the prediction of $f_{\max}$ was examined, after making each of the assumptions leading to the three expressions for τ_{eff}. For the first two, the error in $f_{\max}$ is less than 1 % over the

range of resistances shown in Fig. 6 (a). Fig. 6 (b) depicts the case after, additonally, making assumption Eq. (17), and shows that the error is greatest at large R_c. This is because the approximated term, $(g_m+2g_{ds}) \rightarrow g_m$ in simplifying Eq. (16), is multiplied by the square of R_c, whereas R_g appears without exponentiation. Fig. 6 indicates that the compact expressions are useful over a wide range of resistance values.

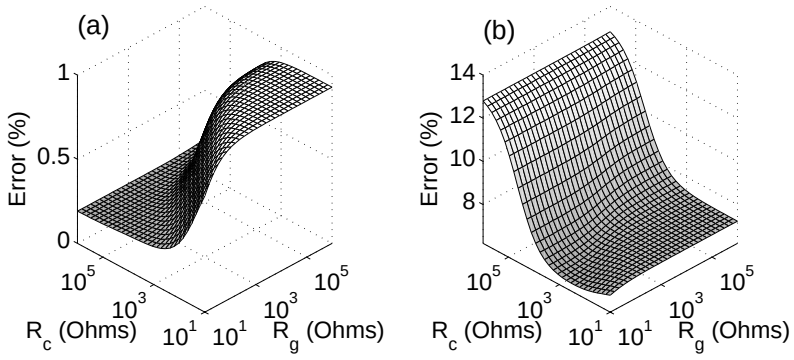

Figure 6. Error in $f_{\max}$ prediction for Device 1, incurred by the use of: (a) Eq. (16); (b) Eq. (18). $V_{DS} = -0.5\,\mathrm{V}$.

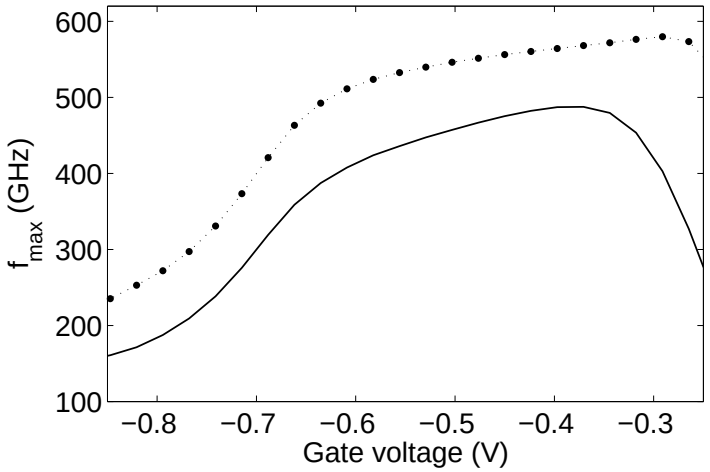

Figure 7. $f_{\max}$ for Device 1 and $f_{\max}$ improvement for Device 1 computed from Eq. (9) without assumptions, both at $V_{DS} = -0.5\,\mathrm{V}$. Solid line: Device 1 as originally specified; dotted line: Device 1 with $t_{\mathrm{ins}} = 8\,\mathrm{nm}$, $L_c = 30\,\mathrm{nm}$, $L_{us} = 5\,\mathrm{nm}$, and $L_{ud} = 15\,\mathrm{nm}$.

Finally, we demonstrate the utility of the compact expressions in guiding design towards CNFETs that should lead to improved $f_{\max}$. Obviously, reducing C_{gd} would be helpful because of its domination of the output admittance. Eqs. (16) and (18) highlight this by elucidating the direct dependence of τ_{eff} on C_{gd}. By contrast, τ_{eff} has a lesser dependence on transconductance. One way to trade-off g_m against C_{gd} would be to increase t_{ins}. Ways to reduce C_{gd} directly would be to

shorten the drain contact L_c, and to increase the gate-drain underlap L_{ud}. Although the functional dependencies of g_m and C_{gd} on $t_{\rm ins}$ and L_{ud} are not readily attainable, the beneficial effect to Device 1 of making these changes is illustrated in Fig. 7, where the peak value of $f_{\max}$ is raised by about 15 % to 580 GHz.

4. CONCLUSIONS

From this study of the extrapolated $f_{\max}$ in Schottky-barrier CNFETs it can be concluded that:

(i) compact expressions for $f_{\max}$ can be derived that are useful over wide ranges of physical properties, parasitic resistances and gate biases;

(ii) the compact expressions provide a useful guide to the design of high-frequency devices;

(iii) $f_{\max}$ values in excess of 0.5 THz should be realizable.

Acknowledgement

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