ELECTROSTATICS OF PARTIALLY GATED CARBON NANOTUBE FETs

J.P. Clifford, D.L. John, *Student Member, IEEE*, L.C. Castro, and D.L. Pulfrey, *Fellow*, *IEEE*

Department of Electrical and Computer Engineering University of British Columbia Vancouver, BC V6T 1Z4, Canada *contact:* pulfrey@ece.ubc.ca or jasonc@ece.ubc.ca

ABSTRACT

The finite-element method is used to solve Poisson's equation, under equilibrium conditions, for coaxial carbon nanotube field-effect transistors in which the gate electrode does not entirely cover the nanotube channel between the source- and drain-end contacts. A conformal transformation is applied to overcome the problems that arise in this open structure of specifying boundary conditions and of terminating the model space. The effect on the potential distribution within the transistor of changing various geometrical properties of the device is investigated, and some special conditions under which appropriate boundary conditions may be defined *a priori* are identified. The effects on the potential energy profile along the nanotube of varying the work function of the end contacts, and of introducing charge into the gate dielectric are also investigated. The latter is shown to be effective in suppressing the otherwise dominant role that the end contacts play in determining the barrier to charge flow in the nanotube, thereby allowing bulk control to occur.

1 INTRODUCTION

Prototype carbon nanotube field-effect transistors (CNFETs) use gates that either fully or partially cover the nanotube channel between metallic source and drain contacts. These contacts act as Schottky barriers, and there is experimental evidence that the barriers can be represented by a simple phenomenological model involving the work function of the contacts [1]. For the case of gates that fully cover the channel, there is strong electrostatic coupling between the gate and the regions of the nanotube close to the end contacts. This leads to gate modulation of the widths of the potential barriers close to the source and drain. Depending on the work function difference between the contact metals and the nanotube, and on the carrier type being considered, these barriers can be either tunneling or thermionic in nature [2]. In recognition of this interfacial control of the current, such devices are labeled Schottky-barrier (SB) CNFETs [3]. When the gate does not extend to the contacts, electrostatic coupling between the gate and the nanotube near the contacts is reduced, resulting in significantly thicker barriers, which will have a detrimental effect on those devices for which tunneling is important. It is possible to reduce the thickness of these barriers in partially gated devices with an additional agent, other than the gate-source voltage, V_{GS} , which is able to influence the potential profiles in the ungated regions near the end contacts. Such devices have been demonstrated, using agents such as: a secondary electrode between the gate and end contacts [4]; a dielectric layer, covering the entire nanotube, and containing substantial fixed negative charge [5]. In both cases, the effect is to dramatically thin the potential barriers at the end contacts to such an extent that they cease to play a major role in current control. Instead, the potential in the body of the device modulates the current, which has led to these devices being labeled as bulk-switched CNFETs [4].

Prototype carbon nanotube field-effect transistors (CNFETs) are presently planar in nature, but ultimate performance is likely to be reached by employing a coaxial geometry [6]. Coaxial structures have not yet been realized in practice, but they have been the subject of several theoretical investigations that have attempted to establish performance limits [7, 8, 9]. Practically, CNFETs are electrostatically open structures due to the presence of gaps between the source/drain and the gate contacts. This is required to keep the contacts electrically separate, and may be realized by utilizing a partially-gated structure with large source/drain contacts, or by using a well-registered gate to "needle" source/drain contacts. Such needle contacts would give higher fields at the ends of the nanotube, which may be advantageous for carrier transport [3]. In both cases, open boundaries exist. These preclude the attainment of an analytical solution for the electrostatics, which is possible in a closed, coaxial geometry [2], and, furthermore, raise the question of how to terminate the model space. Recent work dealing with the electrostatics of related structures has not given details of how this question may be answered [10, 11]. Termination could be achieved by seeking regions in which Neumann boundary conditions, preferably with the normal component of the electric field set to zero, can be applied. These regions are hard to find a priori, without either increasing the model space to such an extent that computational time becomes excessive, or distorting the electrodes from a realistic form.

In this paper, we provide a general solution for the potential distribution in coaxial structures by applying the technique of conformal mapping to allow termination of the model space in a tractable manner, without having to resort to the imposition of artificial boundary conditions. The influence on the potential profiles within the model space of key device parameters, such as: gate-contact spacing; metalization thickness; end-contact radius; end-contact work function; and dielectric charge, is studied. By investigating the equilibriium longitudinal potential profiles on the nanotube in these various devices, some information on the relationship between the physical properties and the current-control mechanism in PG-CNFETs can be inferred.

2 THE MODEL

A coaxial CNFET structure, such as that shown in Fig. 1, has azimuthal symmetry, so the electrostatic problem reduces to solving a two-dimensional Poisson equation self-consistently with the charge in the system. The charge on the surface of the nanotube is computed as already described in detail for the case of fully gated SB-CNFETs [2]. Briefly, the local electrostatic potential is allowed to rigidly shift the nanotube density-of-states, which is computed using the nearest-neighbour tight-binding approximation. The degeneracy of the energy bands is taken into account, Fermi-Dirac statistics are used, and both electrons and holes are

considered. The self-consistent solution is effected using a standard finite-element package¹.

The open boundary problem is solved using the method of Ref. [12] where the solution domain is split into two subdomains: a central disk of radius R_B that encloses all of the contacts and the nanotube; and the region outside of this disk. If we exploit the azimuthal symmetry in the problem, the appropriate far-field equation is

$$\frac{\partial^2 V}{\partial s^2} + \frac{1}{s} \frac{\partial V}{\partial s} + \frac{\partial^2 V}{\partial z^2} = 0, \tag{1}$$

where the boundary between the two subdomains introduces a matching condition where we require that V be continuous and smooth.

The outer region may be solved using a conformal mapping that transforms it into another disk. If u = z + is and $t = \zeta + i\sigma$ represent the coordinates in the untransformed and transformed domains, respectively, the appropriate mapping is

$$t = \frac{R_B^2}{u}.$$
 (2)

This transformation is convenient since the transformed domain is of the same size and shape as the untransformed domain. Applying this transformation to Eq. (1) yields

$$\left(\zeta^2 + \sigma^2\right) \left(\frac{\partial^2 \bar{V}}{\partial \zeta^2} + \frac{\partial^2 \bar{V}}{\partial \sigma^2}\right) - 2\zeta \frac{\partial \bar{V}}{\partial \zeta} + \left(\frac{\zeta^2 - \sigma^2}{\sigma}\right) \frac{\partial \bar{V}}{\partial \sigma} = 0 \tag{3}$$

subject to the matching condition mentioned previously, and where the overbar indicates that the potential is in the transformed coordinate system.

The continuity condition is easily satisfied on both boundaries since the mapping does not change the value of V, it merely changes the coordinate representation. The smoothness condition may be satisfied by noting that

$$\frac{\partial V}{\partial s} = \frac{1}{R_B^2} \left(2\sigma \zeta \frac{\partial \bar{V}}{\partial \zeta} - \left(\zeta^2 - \sigma^2\right) \frac{\partial \bar{V}}{\partial \sigma} \right),\tag{4}$$

$$\frac{\partial V}{\partial z} = -\frac{1}{R_B^2} \left(\left(\zeta^2 - \sigma^2 \right) \frac{\partial \bar{V}}{\partial \zeta} + 2\sigma \zeta \frac{\partial \bar{V}}{\partial \sigma} \right).$$
(5)

This implies that the smoothness condition is given by

$$\nabla_u V \cdot \hat{n}_u = -\nabla_t \bar{V} \cdot \hat{n}_t,\tag{6}$$

where ∇_u and ∇_t are the gradient operators in the untransformed and transformed domains, respectively, and \hat{n}_u and \hat{n}_t are the unit outward normals to those domains.

In short, the open boundary problem has been reformulated as two coupled closed boundary problems with a continuous and smooth solution across the boundaries. This reformulated problem lends itself well to the finite element technique for solution.

¹FEMLAB, see *http://www.comsol.com*

3 RESULTS

To examine the effect of critical device features on the electrostatics of PG-CNFETs, we begin with defining a baseline device in which, with respect to Fig. 1, L_{gap} is 500 nm and the metal thicknesses T_{gate} and R_{contact} are 50 nm. Then, we systematically vary key device parameters, as listed in Table 1. The lengths of the end contacts, L_{contact} , and of the nanotube, $(=L_{\text{gate}} + 2L_{\text{gap}})$, are set to 1000 nm and 2000 nm, respectively. Simulations were performed for an intrinsic (16,0) nanotube, for which the radius, bandgap and work function are 0.63 nm, 0.62 eV and 4.5 eV [13], respectively. Unless otherwise stated, the work function of the gate is taken to be 4.5 eV. The relative permittivity of the gate dielectric is 25, as is appropriate for zirconia [5], and the dielectric thickness is 8 nm. The relative permittivity for the space within the nanotube is taken to be unity [14]. Results were obtained for equilibrium conditions ($V_{DS} = 0$), and, unless otherwise stated, with $V_{GS} = 0.5$ V. The dielectric properties and the values of L_{gap} and T_{gate} that are considered here have been used in experimental devices [5], and they provide a useful starting point for our general analysis. However, note that the device specified in Ref. [5] was planar, not coaxial, and a larger diameter tube was used, so the results presented here are not meant to precisely model that particular device. In all the

Device	$L_{\rm gap}$	$R_{\rm contact}$	T_{gate}	$Q_{ m ins}$	$\Phi_{S,D}$
	nm	nm	nm	$charges/nm^3$	eV
Baseline	500	50	50	0	4.50
Thick metallization	500	250	250	0	4.50
Small gap	100	50	50	0	4.50
Needle contact	500	0.63	50	0	4.50
Low work function	500	50	50	0	4.18
Charged dielectric	500	50	50	-0.1	4.50

Table 1: PG-CNFET devices and parameters studied in this work. See Fig. 1 for the meaning of the device-dimension symbols. Q_{ins} is the volumetric density of charge trapped in the gate dielectric, $\Phi_{S,D}$ is the work function of the source- and drain-end contacts.

cases simulated, the radius R_B of the boundary between the "real" space and the conformed space (see Eq.(2)) was taken to be slightly larger than the minimum possible to encompass the actual device. Simulations performed with larger values of R_B did not change the final results within the limits of accuracy of the solution.

Equipotential plots are shown in Fig. 2 for the devices specified in the first four rows of Table 1. The plots show the edges of the source and gate electrodes on the left and right, respectively, and the region of interest between them. In view of the symmetry of the structure in the longitudinal direction about the centre of the gate electrode, similar potential distributions will exist in the region between the gate and the drain. Firstly, let us concentrate on the free-space region between the gate and source electrodes. The appearance within this space of parallel equipotentials would indicate a perpendicular path along which it would be possible to specify a simple, homogeneous Neumann boundary condition, thereby allowing for the possibility of a straightforward electrostatic solution, e.g., one that did not require conformal mapping. Ideally, the equipotential lines crossing a longitudinal path between the source and gate electrodes would have only a radial component, allowing the radial field E_s , *i.e.*, the field in the s-direction in Fig. 1, to be set to zero. For the baseline case, Fig. 2(a), it is clear that there is no such simple path; the aspect ratio, $(R_{\text{contact}}/L_{\text{gap}})$ or $(T_{\text{gate}}/L_{\text{gap}})$, is too small for E_s to be ignored. Increasing the aspect ratio, either by thickening the metallization, as in Fig. 2(b), or by shortening the gap, as in Fig. 2(c), gives the expected result of a more dominant longitudinal field. In each of these latter examples, a homogeneous Neumann boundary condition could probably be applied with impunity, *e.g.*, along a longitudinal path at a radius of about one-half of the metal thickness.

Conversely, it follows that a reduction of R_{contact} , with respect to the baseline case, will give the opposite result. This case is of interest, particularly in the limit of R_{contact} approaching the radius of the nanotube, as it could be realized by having the source and drain made from metallic nanotubes. Such tubes could also form the interconnects between transistors, raising the interesting spectre of nanoscale integrated circuits of an entirely different form from that of silicon ICs [15]. Fig. 2(d) shows the equipotential plot for the case of essentially equaldiameter metallic and semiconducting tubes. The radial field is pronounced over nearly all the free-space region in the vicinity of the uncovered dielectric surface. Thus, in summary, Fig. 2 highlights the importance of the metallization/gap aspect ratio in determining the effort that needs to be put into obtaining a correct electrostatic solution.

Turning now to the equilibrium energy band diagrams of the actual nanotubes in the four cases just discussed, results are presented in Fig. 3. Note that these devices have positive barrier-height contacts at the source and drain. Because of the symmetry of the bands in equilibrium, and to facilitate the discussion of electron and hole injection, the conduction band is shown only at the source end of the tube (Fig. 3(a)), and the valence band only at the drain end of the tube (Fig. 3(b)). In the baseline case, the conduction-band profile at the source end of the device indicates a thick tunneling barrier. This would form a serious impediment to electron injection from the source. At the drain end, there is a large barrier to thermionic emission of holes into the tube. Thus, the prospects for useful FET operation, either in the *n*-type or *p*-type conduction modes, are not promising for the baseline device. Increasing the thickness of the metallization of all the electrodes by a factor of 5 does not alter this general conclusion, although Fig. 3 does indicate some interesting behaviour. Near to the source electrode, for example, the barrier is slightly thicker than in the baseline case. This is due to the well-documented fact that the electrostatic influence of the end contact extends into the tube to a distance that is directly related to the radius of the contact [3]. Near the edge of the gate electrode, however, the potential barrier becomes thinner than in the baseline case. This interesting feature is likely due to the manner in which the potential at the sidewalls of the gate electrode couples to the nanotube. If the gate electrode is very thin, the field will be focussed around the thin edge, and hence band-bending should occur close to that edge. For a thick contact, the field is not as focussed, so we see the effect of the gate over a longer length scale. In terms of a possibly useful positive-barrier device, Fig. 3(a) indicates that the ungated region must be made smaller than the 500 nm used in the devices discussed above. An example of a relatively narrow interfacial barrier, which may allow some tunneling, is shown for the case of $L_{gap} = 100 \text{ nm}$.

We now examine the case of a zero barrier-height contact by setting the source/drain work functions to 4.18 eV, as specified in row 5 of Table 1. Results are shown in Fig. 4. The lower work-function difference at the source allows a greater number of electrons to be thermionically emitted over the large barrier near that contact. At the drain contact, the barrier is either too thick for tunneling, or too high for significant thermionic emission. Thus, we consider the effect on this *n*-type device of increasing V_{GS} . Initially, up to $V_{GS} = 0.25$ V (see Fig. 4), the gate does exercise bulk-control over the potential barrier. But, thereafter, the barrier is determined more by the source metallization properties, namely, geometry and work function. This is a consequence of the large value of L_{gap} considered here, which ensures that the potential in the vicinity of the source contact is not well coupled to the gate potential.

We now consider the effect on the equilibrium electrostatics of allowing a volumetric charge density to exist within the gate dielectric material. Sizable charge densities may arise, for example, from incorporation of oxidative species into the dielectric during deposition of zirconia from a chloride precursor [5]. An upper limit of 1 atom% of chloride ion incorporation has been suggested, which translates to about 0.8 ions/nm^3 . Here we take a more conservative number of 0.1 ions/nm^3 as we find that this is sufficient to give a large effect. This case is specified in row 6 of Table 1. The charge trapped in the dielectric induces hole "doping" in the nanotube, and has a dramatic effect on the equilibrium band diagram, as can be seen from Fig. 5(a). The massive hole charge induced in the nanotube by the charge in the dielectric raises the energy of the bands in the gap between the gate and the end contacts. This has the effect of "stretching" the band edges of the nanotube at the contacts so that inter-band tunneling is facilitated [16], thereby rendering the contacts essentially ohmic. The charge in the ungated portion of the dielectric essentially isolates the gate from the end contacts, so application of V_{GS} serves only to influence the nanotube potential in the region directly under the gate. Taking $V_{GS} = 1.3$ V as a reference point, Fig. 5(a) shows the effect of changing V_{GS} to 0.9 V, whereas Fig. 5(b) shows the effect of changing V_{GS} to 1.6 V. The reference value of 1.3 V was chosen because it represents, for the particular case under study, the situation of the gate-covered portion of the nanotube being intrinsic, *i.e.*, the electrons induced by the positive gate voltage compensate the holes induced by the negative charge in the dielectric. Application of a lower V_{GS} leads to a *p*-type device, whereas application of a higher V_{GS} leads to an *n*-type device. In the former case, application of $V_{DS} < 0$ could allow hole flow via inter-band tunneling at the drain contact, whereas, in the latter case, application of $V_{DS} > 0$ could allow electron flow via inter-band tunneling at the source contact. Similar end results of ambipolar conduction have been observed in planar, fully-gated CNFETs [17, 18], and in these cases the transformation in device type has been postulated as being due to process-induced changes in the work functions of the end contacts. In the PG-CNFET considered here, the work function of the end contacts is irrelevant because of the extreme band-bending caused by the charge in the dielectric. However, process-induced changes in the work function of the gate could be important because the potential on the gate is actually $(V_{GS} - \Phi_G)$ [2]. Thus, the change in V_{GS} of 0.7 V, *i.e.*, appoximately the bandgap of the nanotube, which is necessary to convert the *p*-type device of Fig. 5(a) to the *n*-type device of Fig. 5(b), could equally well be due to a change in Φ_G . This offers an alternative explanation for the type change noted for the PG-CNFET in Ref. [5], where the effect of hydrogen annealing was postulated to change the work functions of the end contacts.

4 CONCLUSIONS

From this work on the electrostatics of partially gated, coaxial carbon nanotube FETs, it can be concluded that:

- 1. the problem of terminating the model space for coaxial carbon nanotube FETs with open boundaries can be overcome by application of an appropriate conformal transformation;
- 2. the aspect ratio of metallization thickness to gap length plays a major role in determining whether homogeneous Neumann boundary conditions can be applied *a priori*;
- 3. for devices with a large separation between the end contacts and the gate (of the order of hundreds of nanometres, as considered here), the gate exerts little influence on the transport-controlling potential barriers at the end contacts;
- 4. an exception to the above arises when charge trapped in the gate dielectric bends the bands at the ends of the nanotubes sufficiently to render the end contacts essentially transparent;
- 5. the conversion of some prototype devices, in which there is substantial negative charge in the dielectric, from p-type to n-type could be due to a process-induced change of the gate work function.

ACKNOWLEDGEMENT

The financial support of NSERC is gratefully acknowledged.

References

- A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, 424, 654–657 (2003).
- [2] D.L. John, L.C. Castro, J.P. Clifford, and D.L. Pulfrey, "Electrostatics of coaxial Schottky-barrier nanotube field-effect transistors," *IEEE Trans. Nanotechnol.*, 2(3), 175– 180 (2003).
- [3] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, "Carbon nanotubes as Schottky barrier transistors," *Phys. Rev. Lett.*, 89(10), 106801–1–106801–4 (2002).
- [4] S.J. Wind, J. Appenzeller, and Ph. Avouris, "Lateral scaling in carbon-nanotube fieldeffect transistors," *Phys. Rev. Lett.*, **91**(5), 058301–1–058301–4 (2003).
- [5] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, and H. Dai, "High-κ dielectrics for advanced carbon-nanotube transistors and logic gates," *Nature Materials*, 1, 241–246 (2002).
- [6] J. Guo, S. Goasguen, M. Lundstrom, and S. Datta, "Metal-insulator-semiconductor electrostatics of carbon nanotubes," *Appl. Phys. Lett.*, 81(8), 1486–1488 (2002).
- [7] J. Guo, M. Lundstrom, and S. Datta, "Performance projections for ballistic carbon nanotube field-effect transistors," Appl. Phys. Lett., 80(17), 3192–3194 (2002).
- [8] J. Guo, A. Javey, H. Dai, S. Datta, and M. Lundstrom, "Predicted performance advantages of carbon nanotube transistors with doped nanotubes as source/drain," *Appl. Phys. Lett.* (2003). Submitted.
- [9] L.C. Castro, D.L. John, and D.L. Pulfrey, "Carbon nanotube transistors: an evaluation," Proc. SPIE Intl. Symp. Microelectronics, MEMS, and Nanotechnology (2003). [Online.] Available: http://nano.ece.ubc.ca.
- [10] S. Heinze, J. Tersoff, and Ph. Avouris, "Electrostatic engineering of nanotube transistors for improved performance," Appl. Phys. Lett., 83(24), 5038–5040 (2003).
- [11] J. Guo, J. Wang, E. Polizzi, S. Datta, and M. Lundstrom, "Electrostatics of nanowire transistors," *IEEE Trans. Nanotechnol.* (2003). In press.
- [12] E.M. Freeman and D.M. Lowther, "A novel mapping technique for open boundary finite element solutions to Poisson's equation," *IEEE Trans. Magn.*, 24(6), 2934–2936 (1988).
- [13] S.J. Tans, A.R.M. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature*, **393**, 49–52 (1998).
- [14] F. Léonard and J. Tersoff, "Dielectric response of semiconducting carbon nanotubes," Appl. Phys. Lett., 81(25), 4835–4837 (2002).

- [15] P.G. Collins and Ph. Avouris, "Nanotubes for electronics," Sci. Am., 62–69 (2000).
- [16] F. Léonard and J. Tersoff, "Negative differential resistance in nanotube devices," Phys. Rev. Lett., 85(22), 4767–4770 (2000).
- [17] R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K.K. Chan, J. Tersoff, and Ph. Avouris, "Ambipolar electrical transport in semiconducting single-wall carbon nanotubes," *Phys. Rev. Lett.*, 87(25), 256805–1–256805–4 (2001).
- [18] R. Martel, V. Derycke, J. Appenzeller, S. Wind, and Ph. Avouris, "Carbon nanotube field-effect transistors and logic circuits," *Proc. Design Automation Conference*, 94–98 (2002).

List of Figures

1	PG-CNFET device structure.	11
2	Equipotential plots for the PG-CNFETs listed in the first four rows of Table 1	
	for $V_{GS} = 0.5$ V. The equipotential contours are at intervals of 24 mV. The	
	source is on the left, and the gate is on the right. The dielectric between the	
	source and gate is visible at the bottom of each figure, but the nanotube is too	
	narrow to be discernible.	11
3	Energy-band diagrams for the devices described in the first four rows of Table 1.	
	The energy is measured with respect to the Fermi level at the end contacts. (a)	
	The conduction-band profile at the source end. (b) The valence-band profile at	
	the drain end	12
4	Energy-band diagrams for the low-work-function device described in the fifth	
	row of Table 1. The energy is measured with respect to the Fermi level at the	
	end contacts (dotted line). The parameter is V_{GS} , and it ranges from 0 (top	
	line) to 0.75 V (bottom line) in increments of 0.25 V . (a) The conduction-band	
	profile at the source end. (b) The valence-band profile at the drain end	13
5	Energy-band diagrams for the PG-CNFET of Ref. $[5]$. (a) Operating as a p -	
	type device, being in the ON state at $V_{GS} = 0.9 \text{ V}$, and the OFF state at 1.3 V .	
	(b) Operating as an <i>n</i> -type device at $V_{GS} = 1.3 \text{ V}$, and being turned ON with	
	a gate work function change from 4.5 to $4.2 \mathrm{eV}$.	14



Figure 1: PG-CNFET device structure.



Figure 2: Equipotential plots for the PG-CNFETs listed in the first four rows of Table 1 for $V_{GS} = 0.5$ V. The equipotential contours are at intervals of 24 mV. The source is on the left, and the gate is on the right. The dielectric between the source and gate is visible at the bottom of each figure, but the nanotube is too narrow to be discernible.



Figure 3: Energy-band diagrams for the devices described in the first four rows of Table 1. The energy is measured with respect to the Fermi level at the end contacts. (a) The conductionband profile at the source end. (b) The valence-band profile at the drain end.



Figure 4: Energy-band diagrams for the low-work-function device described in the fifth row of Table 1. The energy is measured with respect to the Fermi level at the end contacts (dotted line). The parameter is V_{GS} , and it ranges from 0 (top line) to 0.75 V (bottom line) in increments of 0.25 V. (a) The conduction-band profile at the source end. (b) The valence-band profile at the drain end.



Figure 5: Energy-band diagrams for the PG-CNFET of Ref. [5]. (a) Operating as a *p*-type device, being in the ON state at $V_{GS} = 0.9$ V, and the OFF state at 1.3 V. (b) Operating as an *n*-type device at $V_{GS} = 1.3$ V, and being turned ON with a gate work function change from 4.5 to 4.2 eV.